WHAT IS CLAIMED IS:

1. A method for correcting a burst of errors having a length of b bits together with a random error, comprising:

providing a received word in a syndrome register for analysis, the syndrome register being defined by a polynomial of degree n-k generating a cyclic code of length n and dimension k, k being the number of information bits in each codeword of said code, the received word being shifted in a first direction in the syndrome register M times, wherein M is less than or equal to n;

analyzing the syndrome register to determine whether the first n-k-b bits in the syndrome register are zero;

when a bit in the first n-k-b bits in the syndrome register is determined to be non-zero, XORing the vector in the syndrome register with all possible syndromes corresponding to one error; and

identifying a random error and an error burst in the last b bits of the syndrome register when an XOR of the first n-k-b bits in the syndrome register results in the first n-k-b bits equaling zero.

2. The method of claim 1, wherein the cyclic code is a shortened cyclic code.

3. The method of claim 1 further comprising determining that the last b bits in the register are a burst corresponding to the last b bits of the burst when the first n-k-b bits in the syndrome register are zero.

4. The method of claim 3 further comprising correcting the burst and restoring the corrected word by shifting the syndrome register M times in a direction opposite to the first direction.

5. The method of claim 1 further comprising when the XORing the syndrome register with all possible syndromes corresponding to one error does not render the first n-k-b bits zero and when the number of shifts of the syndrome register for the received word, M, is less than n, shifting the syndrome register and repeating the analyzing the syndrome register.

6. The method of claim 1, wherein after identifying a random error and an error burst in the last b bits of the syndrome register, correcting the burst and restoring the corrected word by shifting the syndrome register M times in a direction opposite to the first direction.

7. The method of claim 1 further comprising declaring an uncorrectable error when M equals n, when an XOR of the first n-k-b bits in the syndrome register does not result in the first n-k-b bits equaling zero and no correction is effected:

8. The method of claim 1, wherein the error burst length, b, is two.

9. The method of claim 1, wherein the error burst length, b, is three.

10. An apparatus for correcting a burst of errors having a length b together with a random error, comprising:

a trap decoder comprising a syndrome register and a buffer register, the syndrome register defined by a polynomial of degree n-k generating a cyclic code of length n and dimension k, k being the number of information bits in each codeword of said code, the received word being shifted in a first direction in the syndrome register M times, wherein M is less than or equal to n; and

a module, coupled to the syndrome register, for determining, for each shift of the received word, whether a bit in the first n-k-b bits in the syndrome register is non-zero, XORing a vector in the syndrome register with all possible syndromes corresponding to one error and identifying a random error and an error burst in the last b bits of the syndrome register when an XOR of the first n-k-b bits in the syndrome register results in the first n-k-b bits equaling zero.

11. The apparatus of claim 10, wherein the cyclic code is a shortened cyclic code.

12. The apparatus of claim 10, wherein the module is further configured for determining that the last b bits in the register are a burst corresponding to the last b bits of the burst when the first n-k-b bits in the syndrome register are zero.

13. The apparatus of claim 12 wherein the module is further configured for correcting the burst and restoring the corrected word by shifting the syndrome register M times in a direction opposite to the first direction.

14. The apparatus of claim 10, wherein the module is further configured for shifting the syndrome register and repeating the analyzing the syndrome register when the XORing the syndrome register with all possible syndromes corresponding to one error does not render the first n-k-b bits zero and when the number of shifts of the syndrome register for the received word, M, is less than n.

15. The apparatus of claim 10, wherein after the module identifies a random error and an error burst in the last b bits of the syndrome register, the module is further configured for correcting the burst and restoring the corrected word by causing the syndrome register to be shifted M times in a direction opposite to the first direction.

16. The apparatus of claim 10, wherein the module declares an uncorrectable error when M equals n, when an XOR of the first n-k-b bits in the syndrome register does not result in the first n-k-b bits equaling zero and no correction is effected:

17. The apparatus of claim 10, wherein the error burst length, b, is two.

18. The apparatus of claim 10, wherein the error burst length, b, is three.

19. An apparatus for correcting a burst of errors having a length b together with a random error, comprising:

memory for receiving a word representing bits of received data; and

a processor, coupled to the memory, the processor being configured for calculating an n-k bit syndrome for each shift of the received word defined by a polynomial of degree n-k generating a cyclic code of length n and dimension k, k being the number of information bits in each codeword of said code, the received word being shifted in a first direction in the syndrome register M times, wherein M is less than or equal to n, the processor determining, for each shift of the received word, whether a bit in the first n-k-b bits in the syndrome register is non-zero, XORing a vector in the syndrome register with all possible syndromes corresponding to one error and identifying a random error and an error burst in the last b bits of the syndrome register when an XOR of the first n-k-b bits in the syndrome register results in the first n-k-b bits equaling zero.

20. The apparatus of claim 19, wherein the cyclic code is a shortened cyclic code.

21. The apparatus of claim 19, wherein the processor is further configured for determining that the last b bits in the register are a burst corresponding to the last b bits of the burst when the first n-k-b bits in the syndrome register are zero.

22. The apparatus of claim 21 wherein the processor is further configured for correcting the burst and restoring the corrected word by shifting the syndrome register M times in a direction opposite to the first direction.

23. The apparatus of claim 19, wherein the processor is further configured for shifting the syndrome register and repeating the analyzing the syndrome register when the XORing the syndrome register with all possible syndromes corresponding to one error does not render the first n-k-b bits zero and when the number of shifts of the syndrome register for the received word, M, is less than n.

24. The apparatus of claim 19, wherein after the processor identifies a random error and an error burst in the last b bits of the syndrome register, the processor is further configured for correcting the burst and restoring the corrected word by causing the syndrome register to be shifted M times in a direction opposite to the first direction.

25. The apparatus of claim 19, wherein the processor declares an uncorrectable error when M equals n, when an XOR of the first n-k-b bits in the syndrome register does not result in the first n-k-b bits equaling zero and no correction is effected:

26. The apparatus of claim 19, wherein the error burst length, b, is two.

27. The apparatus of claim 19, wherein the error burst length, b, is three.

28. A storage system, comprising:

at least one magnetic recording medium for recording data thereon;

at least one transducer, associated with each of the at least one magnetic recording medium, for reading and writing data on the magnetic recording medium;

a motor, coupled to the at least one magnetic recording medium, for translating the magnetic recording medium;

an actuator, coupled to the transducer, for translating the at least one transducer relative to the at least one magnetic recording medium; and

a storage device signal processor, coupled to the motor, transducer and actuator, for controlling the operation of the motor and actuator and for correcting a burst of errors having a length b together with a random error in a word received from the transducer, the storage device signal processor being configured for calculating an n-k bit syndrome for each shift of the received word defined by a polynomial of degree n-k generating a cyclic code of length n and dimension k, k being the number of information bits in each codeword of said code, the received word being shifted in a first direction in the syndrome register M times, wherein M is less than or equal to n, the processor determining, for each shift of the received word, whether a bit in the first n-k-b bits in the syndrome register is non-zero, XORing a vector in the syndrome register with all possible syndromes corresponding to one error and identifying a random error and an error burst in the last b bits of the syndrome register when an XOR of the first n-k-b bits in the syndrome register results in the first n-k-b bits equaling zero.

29. A program storage device readable by a computer, the program storage device tangibly embodying one or more programs of instructions executable by the computer to perform a method for correcting a burst of errors together with a random error using shortened cyclic codes, the method comprising:

providing a received word in a syndrome register for analysis, the syndrome register being defined by a polynomial of degree n-k generating a cyclic or shortened cyclic code of length n and dimension k, k being the number of information bits in each codeword of said code, the received word being shifted in a first direction in the syndrome register M times, wherein M is less than or equal to n;

analyzing the syndrome register to determine whether the first n-k-b bits in the syndrome register are zero;

when a bit in the first n-k-b bits in the syndrome register is determined to be non-zero, XORing the vector in the syndrome register with all possible syndromes corresponding to one error; and

identifying a random error and an error burst in the last b bits of the syndrome register when an XOR of the first n-k-b bits in the syndrome register results in the first n-k-b bits equaling zero.

30. An apparatus for correcting a burst of errors having length b together with a random error, comprising:

means for receiving a word representing bits of received data;

means, coupled to the memory, for calculating an n-k bit syndrome for each shift of the received word defined by a polynomial of degree n-k generating a cyclic code of length n and dimension k, k being the number of information bits in each codeword of said code, the received word being shifted in a first direction in the syndrome register M times, wherein M is less than or equal to n;

means for determining for each shift of the received word, whether a bit in the first n-k-b bits in the syndrome register is non-zero;

means for XORing a vector in the syndrome register with all possible syndromes corresponding to one error; and

means for identifying a random error and an error burst in the last b bits of the syndrome register when an XOR of the first n-k-b bits in the syndrome register results in the first n-k-b bits equaling zero.